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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
ENCARNACION, YAMIR

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,459	GEFEN ET AL.	
	Examiner	Art Unit	
	Yamir Encarnacion	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-3, 6, 8, 10-12, 14-17, and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by *Honma* (USPN: 5,606,529).

Claimed	***Honma***
1. A system for enabling code execution from non executable memory, comprising:	See figure 2b.
(i) an executing entity, for executing code for a host system;	See figure 2b, the host.
(ii) a non-executable memory component, for storing system code and data; and	See figure 2b, the flash memory 2.

(iii) an executable memory component, for operating as a memory buffer for executing said code, such that a portion of contents of said non-executable memory component is located within said executable memory component, and said portion of contents of said non-executable memory component emulates executable functions of said executable memory component.	See figure 2b, the cache memory 3.

As to claim 1, and the recitations requiring that the "non-executable memory component" store "system code and data," the examiner notes that column 2, lines 30-33 speak of "the temporary saving of program code existing on a main storage to the non-volatile storage medium and the reading of the program code from the non-volatile medium."

As to claim 2, the reference meets the limitation of the claim. See column 3, lines 13-15. Also, see the step labeled "transfer data in flash memory into cache" in figure 1b.

As to claim 3, column 2, line 67 thru column 2, line 1 states that the memory 2 "may be any memory so long as it is an EEPROM).

As to claim 6, see the comments for claims 1 and 2 above.

As to claim 8, the step labeled "read/write request" in figure 1b meets the limitation of "querying said executable memory for data." Also, see the step labeled "transfer data in flash memory into cache" in figure 1b meets the limitation of "when queried address of said data is only available in non-executable memory, initiating a download operation from a required location of said non-executable memory, to a buffer area of said executable memory."

As to claims 10-11, see figure 2b.

As to claim 12, if there is a cache miss, data is transferred from the flash into the cache. See figure 1B.

As to claim 14, the reference meets the limitation of the claim. Column 1, lines 45-48 state that "non-volatile memory [] is made larger in capacity [] than the volatile memory."

As to claims 15-16, see the comments above.

As to claim 17, if a requested portion is not in the volatile memory, it is transferred into the volatile memory from the non-volatile memory. See figure 1b, the step labeled "Transfer Data in Flash Memory into Cache."

As to claims 20-22, the reference meets the limitation of the claim. As to the "first" and "second executable memory" components note the first and second cache blocks.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 8, 10-11, 14-17, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Pashley* (USPN: 6,418,506 B1) in view of *Garvin* (USPN: 6,260,156 B1) or *Alexis* (USPN: 6,260,103 B1).

Claimed	***Pashley***
4. A system for executing code using non-executable memory, comprising:	See figure 1.
(i) An executing entity, for executing code;	See figure 1, the processor 104.
(ii) A non-executable memory component, for storing said code and data; and.	See figure 1, the flash array 103.
(iii) A plurality of executable memory components	See figure 1, the RAM Write Buffer array 101.
that alternate as multiple memory buffers	The examiner notes that the RAM Write buffer array serves (that is, it "alternates") as multiple memory buffers.
for preventing memory lockage for accesses to said data during download operations of said code.	The examiner notes that column 5, lines 10-14, state that "for one embodiment, data is read from the RAM array by an external device during at least a portion of time in which data is written to the flash array from [] the RAM array."

Pashley does not explicitly storing system code in the flash array 103. The examiner takes "Official notice" that it was well known that processors, such as processor 104 executed program code prior to the filing of the present application. The examiner also takes "Official notice" that program code is stored in memory. Given that processor 104 executes program code and that the processor 104 is not shown connected to any other memory other than IC 100, it would have been obvious to a person of ordinary skill in the art the processor 104 obtained its program code from IC 100. Because program code stored in volatile memory 101 would have been lost in the event of a power loss, it would also have been obvious to those of ordinary skill in the art that such code would have had to have been stored in the non-volatile flash array 103 for the purpose of surviving a power loss.

In the alternative, a person of ordinary skill in the art would have found it obvious to store program code in the flash array 103 shown in figure 1 of *Pashley* given that as *Garvin*, column 4, lines 35-38. explains the flash memory can be organized "so that the host system can access the flash memory for storing data, code, or other information" and *Pashley* does not explicitly describe of any other place to put the code information. Similar to *Garvin*, *Alexis* recognized that "flash memory can be used to store both code and data." See *Alexis*, column 1, lines 30-31.

As to claim 5, the reference meets the limitation of the claim.

As to claims 1 and 3, see comments above.

As to claims 2, 6, and 8, see figure 4 and the comments above.

As to claim 10, see the comments for claim 4 above.

As to claim 11, *Pashley* shows IC 100 as separate from processor 104.

As to claim 14, *Pashley*, column 4, lines 56-59 state that "the memory storage capacity of the RAM write buffer array can be made significantly smaller than the storage capacity of the flash array, while still providing more than adequate support for read and write operations to memory."

As to claim 15, see the comments for claims 10 and 11 above.

As to claim 16, see *Pashley*, figure 4, step 435 labeled "Read Target Data From RAM."

As to claim 17, if the memory storage capacity of the RAM write buffer array is significantly smaller than the storage capacity of the flash array, it would necessarily or in the alternative obviously follow that only portions of what was in the flash array could be placed in the RAM write buffer.

As to claims 20-22, the combination meets the limitations of the claims.

5. Claims 7, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Honma, Pashley/Garvin* or *Pashley/Alexis* as applied to claims 6 and 17 above, and further in view of *Shimizu* (USPN: 5,644,535) and *Kikuchi* (USPN: 6,477,632 B1), *Claxton* (USPN: 5,901,293), *Sakamoto* (USPN: 5,303,201).

As to claims 7, 18, and 19, *Honma, Pashley/Garvin* or *Pashley/Alexis* do not explicitly disclose of supplying a busy signal if requested contents are not available such that a read cycle is delayed until the requested contents are available. *Shimizu, Kikuchi, Claxton,* and *Sakamoto* are all examples of memories outputting "ready" signals when requested contents are available. See

Kikuchi, figure 1, the Ready/Busy signal; *Claxton*, figure 1, the Ready/Busy signal; *Shimizu*, figure 1, the RDY signal; *Sakamoto*, figure 2, Rdy/Bsy signal 105. A person of ordinary skill in the art would have found it obvious to incorporate a Ready signal such as the ones described by *Shimizu, Kikuchi*, *Claxton*, and *Sakamoto* into *Honma, Pashley/Garvin* or *Pashley/Alexis* for the purpose of reducing memory cycle time. *Kikuchi*, *Claxton*, and *Sakamoto* are evidence that the Busy signal is the complement of the "Ready" signal and therefore rendered obvious in light of the Ready signal.

6. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Nojima* (USPN: 6,246,634 B1) in view of *Garvin* or *Alexis*.

Claimed	***Nojima***
1. A system for enabling code execution from non executable memory, comprising:	See figure 1.
(i) an executing entity, for executing code for a host system;	Not shown.
(ii) a non-executable memory component, for storing system code and data; and	See figure 1, Flash memory array 12 or Flash memory array 16.

(iii) an executable memory component, for operating as a memory buffer for executing said code, such that a portion of contents of said non-executable memory component is located within said executable memory component, and said portion of contents of said non-executable memory component emulates executable functions of said executable memory component.	See figure 1, SRAM 14 or SRAM 18.

Nojima does not explicitly show an "executing entity." The examiner takes "Official notice" that processors were well known prior to the time of filing of the present application. A person of ordinary skill in the art would have found it obvious to use the memory circuit described by *Nojima* with a processor. Furthermore, those of ordinary skill in the art would have found it obvious to store code in the memory circuit as suggested by *Garvin* or *Alexis* for the purpose of using the memory described by *Nojima* in the conventional manner that memories were used prior to the filing of the present application.

As to claims 7, 18, and 19, note the RDY/BY signal shown in figure 1.

As to claims 9 and 13, see column 4, lines 42-45

Response to Arguments

7. Applicant's arguments filed December 10, 2002 have been fully considered but they are not completely persuasive.

The examiner has re-written the Office Action in view of applicant's comments regarding the storage of executable code in the non-volatile memory. The examiner believes that most of the arguments made by applicant are rendered moot by the rewritten Office Action.

As to applicant's comments that *Honma* deals with "the prior art method of downloading executable code from a nonvolatile memory to the RAM of the host device that is large enough to accommodate the full address range of the executable code," the examiner does not agree with applicant because CPU 9 in *Honma* is not shown as having direct access to any other RAM other than cache memory 3 and the cache memory 3 is smaller than the non volatile memory in the embodiment described in column 1, lines 60-62.

Conclusion

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Yamir Encarnacion by phone at (703) 308-5466.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any formal response to this action intended for entry should be mailed to Commissioner of Patents and Trademarks, Washington, D.C. 20231 or faxed to (703) 746-7239 and labeled "FORMAL" or "OFFICIAL." Any informal or draft communication should be faxed to (703)

746-7240 and labeled "INFORMAL" or "UNOFFICIAL" or "DRAFT" or "PROPOSED" and followed by a phone call to the Examiner at the above number. Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

YEE

Yamir Encarnacion

Patent Examiner

February 12, 2003

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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